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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/893,598	06/29/2001	Yoshinori Uchiyama	01USFP644-M.K.	6524

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EXAMINER	
XIAO, KE	

ART UNIT	PAPER NUMBER
2629	

DATE MAILED: 08/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/893,598	UCHIYAMA, YOSHINORI	
	Examiner	Art Unit	
	Ke Xiao	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 May 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *11-14 and 22* is/are allowed.

6)☒ Claim(s) *1-5,10,15-17,20 and 21* is/are rejected.

7)☒ Claim(s) *6-9,18 and 19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/28/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2 and 21 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Yamaguchi (US 4,672,647).

Regarding independent **Claim 1**, Yamaguchi clearly teaches a semiconductor circuit system (Yamaguchi, Fig. 7a, Col. 5 lines 1-25) comprising:

a first signal line (Yamaguchi, Fig. 7a, element DI1-DIk); and

n circuit sections, where n is an integer greater than 2, each of which includes an input terminal and an output terminal (Yamaguchi, Fig. 7a elements $S_{11\text{-}km}$),

wherein the input terminals of only predetermined k ones of the n circuit sections are connected to the first signal line, where k is an integer equal to or greater than 2 and less than n (Yamaguchi, Fig. 7a elements $S_{11\text{-}k1}$), and

the output terminal of an m^{th} one of the n circuit sections is connected to the input terminal of an $(m+k)^{th}$ one of the n circuit sections, where m is an integer varying between 1 and n-k, thereby k of the n circuit sections are activated at a given time (Yamaguchi, Fig. 7a Q terminals of $S_{11\text{-}k2}$).

Regarding independent **Claim 21**, Yamaguchi clearly teaches a semiconductor system (Yamaguchi, Fig. 7a, Col. 5 lines 1-25) comprising:

n circuit sections (n being an integer >= 2), each of which has an input terminal and an output terminal (Yamaguchi, Fig. 7a $S_{11\text{-}km}$ D and Q terminals),

wherein:

k (k being an integer satisfying 2 <= k < n) of the n circuit sections are started in response to control signals at the input terminal of each of the k circuit sections (Yamaguchi, Fig. 7a elements $S_{11\text{-}k1}$),

the output terminal of an m^{th} one (1 <= m <= n-k) of the n circuit sections is connected to the input terminal of an $(m+k)^{th}$ one of the n circuit sections (Yamaguchi, Fig. 7a elements $S_{11\text{-}k1}$ Q terminals), and

the $(m+k)^{th}$ circuit section is started in response to an output signal outputted from the output terminal of the m^{th} circuit section so that k of the circuit sections are active at a given time (Yamaguchi, Fig. 7a elements $S_{11\text{-}k2}$).

Regarding **Claim 2**, Yamaguchi further teaches that each of the n circuits sections starts an operation in response to a start signal on the first signal line and stops the operation a predetermined time after the start of the operation (Yamaguchi, Fig. 7a element DI1-DIk, when signal in is input into the flip flop the flip flop opens the D terminal to receive the input and closes the D terminal after a predetermined time in order to retain the signal).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaguchi (US 4,672,647).

Regarding **Claim 10**, Yamaguchi fails to teach that the n circuits of Claim 1 are respectively provided on different semiconductor chips. However, Yamaguchi does teach that separating blocks of circuitry on to different semiconductor chips (Yamaguchi, Col. 5 lines 1-25). It would have been obvious to one of ordinary skill in the art at the time of the invention to further separate the circuits of Yamaguchi so that each of the flip flops was on a respective semiconductor chip in order to further modulate the device.

Claims 3-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaguchi (US 4,672,647) in view of the admitted prior art.

Regarding **Claim 3**, Yamaguchi further teaches wherein each of the n circuit sections comprises:

a register circuit (Yamaguchi, Fig. 7a elements $S_{11\text{-}km}$),

Yamaguchi fails to teach that each of the n circuit sections has a differential input circuit, wherein the differential input circuit is activate in response to a start signal on the

first signal line to start an operation stop the operation a predetermined time after the start of the operation.

The applicant's admitted prior art teaches a single circuit block which has a differential input circuit and a register circuit, further it teaches that that the differential input circuit takes an input from a start signal on a first signal line to start an operation and stops the operation after a predetermined time after the start of the operation (Admitted Prior Art, Fig. 3).

It would have been obvious to one of ordinary skill in the art at the time of the invention to replace the flip flops of Yamaguchi with the more complex block circuits of the applicant's admitted prior art in order to adapt the shift registers of Yamaguchi to support display driving. The combined teachings of Yamaguchi in view of the applicant's admitted prior art would then satisfy all the limitations of Claim 3.

Regarding **Claim 4**, Yamaguchi further teaches wherein each of the n circuit sections comprises:

a register circuit (Yamaguchi, Fig. 7a elements $S_{11\text{-}km}$),

Yamaguchi fails to teach that each of the n circuit sections has a differential input circuit, wherein the differential input circuit is activate in response to a start signal on the first signal line to start an operation and stops the operation in response to an output from the register circuit.

The applicant's admitted prior art teaches a single circuit block which has a differential input circuit and a register circuit, further it teaches that that the differential input circuit takes an input from a start signal on a first signal line to start an operation

and stops the operation in response to an output from the register circuit (Admitted Prior Art, Fig. 3) (The differential input circuit is for inputting data into the shift register and when the shift register is outputting the data the input operation of the differential circuits must inherently stop).

It would have been obvious to one of ordinary skill in the art at the time of the invention to replace the flip flops of Yamaguchi with the more complex block circuits of the applicant's admitted prior art in order to adapt the shift registers of Yamaguchi to support display driving. The combined teachings of Yamaguchi in view of the applicant's admitted prior art would then satisfy all the limitations of Claim 4.

Regarding **Claim 5**, the combined teachings of Yamaguchi in view of the admitted prior art teaches that the output from the register circuit is used as the start signal for a next one of the n circuit sections which is connected to the current circuit section (Yamaguchi, Fig. 7a, Admitted Prior Art, Fig. 3).

Claims 15-17 and 20 rejected under 35 U.S.C. 103(a) as being unpatentable over the applicant's admitted prior art in view of Yamaguchi (US 4,672,647).

Regarding independent **Claim 15**, the applicant's admitted prior art teaches a liquid crystal apparatus (Figs. 1-3), comprising:

a liquid crystal display panel (Fig. 1 element 102);

a horizontal drive unit (Fig. 1 element 104); and

a vertical drive unit (Fig. 1 element 103),

wherein the horizontal driver has n circuit blocks and a first signal line (Fig. 2).

The applicant's admitted prior art fails to teach that the circuit blocks are connected together as claimed.

Yamaguchi teaches a shifter register device comprising:

a first signal line; and

n circuit sections, where n is an integer greater than 2, each of the n circuit sections having an input terminal and an output terminal, input terminals of only predetermined k ones of the n circuit sections are connected to the first signal line, where k is an integer equal to or great than 2 and less than n, and the output terminal of an m^{th} one of the n circuit sections is connected to the input terminal of an $(m+k)^{th}$ one of the n circuit sections, where m is an integer varying between 1 and n-k, such that k of the circuit sections are active at a given time (Yamaguchi, Fig. 7a).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modified the connection scheme of the register blocks as taught by the admitted prior art with the connection scheme as taught by Yamaguchi in order to save power (Yamaguchi, Col. 1 line 45 to Col. 2 lines 24).

Regarding **Claim 16**, the combined teaches of the admitted prior art in view of Yamaguchi teaches that each of the n circuit sections starts an operation in response to a start signal on the first signal line and stops the operation a predetermined time after the start of the operation (Yamaguchi, Fig. 7a, Admitted Prior Art, Fig. 3).

Regarding **Claim 17**, the admitted prior art further teaches that each of the n circuit sections includes a differential input circuit and a register circuit (Fig. 3), and

the differential input circuit is activated in response to a start signal on the first signal line to start an operation and stops the operation a predetermined time after the start of the operation (Fig. 3).

Regarding **Claim 20**, the admitted prior art teaches a method of driving a liquid crystal display device having a liquid crystal display panel with a horizontal drive unit and a vertical drive unit, wherein the horizontal drive unit comprises a first signal line and n circuit sections (Figs. 1-3).

Admitted prior art fails to teach that the n circuits are connected together thought input and output terminals as claimed.

Yamaguchi teaches n circuit sections where n is an integer greater than 2, each having an input and an output terminal, wherein the first signal is connected to only predetermined k ones of the n circuit sections, where k is an integer equal to or greater than 2 and less than n; and

connecting the output terminal of an m^{th} one of the n circuit sections to the input terminal of an $(m+k)^{th}$ one of the n circuit sections, where m is an integer varying between 1 and n-k so that k of the n circuit sections are active at a given time (Yamaguchi, Fig. 7a).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modified the connection scheme of the register blocks as taught by the admitted prior art with the connection scheme as taught by Yamaguchi in order to save power (Yamaguchi, Col. 1 line 45 to Col. 2 lines 24).

Allowable Subject Matter

Claims 6-9, 18-19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Statement of reasons for the indication of allowable subject matter:

Regarding **Claims 6 and 18**, prior art fails to show "a control circuit including a latch circuit ... response to the second signal". The closes art is in the applicant's admitted prior art, which does not show a control circuit as claimed.

Regarding **Claims 7-9 and 19**, they are dependent either directly or indirectly from Claims 6 and 18.

Claims 11-14 and 22 are allowed.

The following is an examiner's statement of reasons for allowance:

Regarding independent **Claims 11 and 22**, prior art fails to show "a control circuit including a latch circuit ... response to the second signal". The closes art is in the applicant's admitted prior art, which does not show a control circuit as claimed.

Regarding **Claims 12-14**, they are dependent either directly or indirectly from allowable Claim 11.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

Applicant's arguments filed May 24th, 2006 have been fully considered but they are not persuasive.

Regarding independent **Claim 1**, the applicant argues that Yamaguchi fails to teach "thereby k of said n circuit sections are activated at a given time" and similarly for independent Claims 15, 20 and 21. The examiner respectfully disagrees. The embodiment previously pointed out by the examiner does not teach such a limitation however the embodiment pointed out by the examiner in the current action specifically teaches that limitation (Yamaguchi, Figs. 7a and 7c). As is clearly pointed out by the circuit diagram of 7a and the timing diagram of 7c, "k of the n circuit sections are activated at a given time".

Additionally regarding **Claim 15**, the applicant alleges that the examiner is using improper hindsight when making the combination of AAPA and Yamaguchi. The examiner respectfully disagrees. Yamaguchi merely teaches a power saving shift register and the AAPA teaches the use of the shift register in a display system therefore it would have been obvious to one of ordinary skill in the art to adapt the shift register with the same structure of the AAPA in order to be more easily applied to display technology.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ke Xiao whose telephone number is (571) 272-7776. The examiner can normally be reached on Monday through Friday from 8:30AM to 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on (571) 272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

July 31st, 2006 - kx -

SUMATI LEFKOWITZ
SUPERVISORY PATENT EXAMINER